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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,809	09/19/2003	Sridhar Kumar	010327-007810US	6629

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EXAMINER	
HOANG, HIEU T	

ART UNIT	PAPER NUMBER
2152	

MAIL DATE	DELIVERY MODE
06/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/665,809	KUMAR ET AL.	
	Examiner	Art Unit	
	HIEU T. HOANG	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,8-14,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6, 8-14 and 16-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/28/2008 has been entered.

2. Claims 5, 7, 15 are cancelled.

3. Claims 1-4, 6, 8-14 and 16-17 are pending.

Response to Amendment

4. The U.S.C. 112 rejection has been withdrawn due to the amendment.

Response to Arguments

5. Applicant's arguments have been fully considered but they moot in view of new ground(s) of rejection.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a

patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 12 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Quiles et al. (US 7,065,072, hereafter Quiles).

8. For claim 12, Quiles discloses a method for routing packet data over a communication network using a telecommunications device that includes a plurality of data processors, the method comprising:

- configuring a first set of one or more data processors in the plurality of data processors for a first logical node in the telecommunications device; configuring a second set of one or more data processors in the plurality of data processors for a second logical node in the telecommunications device (fig. 2, each line card is a data processor connected to a slot, col. 4 lines 37-67, line cards belonging to a provider is a logical node, there are 3 logical nodes for 3 providers);
- receiving data associated with the first logical node; routing the data from the telecommunications device to a first destination on the communication network using the one or more data processors in the first logical node; receiving data associated with the second logical node; and routing the data from the telecommunications device to a second destination on the communication network using the one or more data processors in the second logical node (col. 4

lines 39-45 and 58-67, network interface cards route data via line cards associated with each service provider according to data paths).

- managing routing data for the first logical node with a first control processor distinct from the first set of data processors; managing routing data for the second logical node with a second control processor distinct from the second set of data processors (col. 4 lines 39-45 and 58-67, network interface cards route data for each service provider via line cards according to data paths)

9. For claim 16, Quiles further discloses the first control processor manages data routing paths for the first network service provider and the second control processor manages data routing paths for the second network service provider (col. 4 lines 39-45 and 58-67, network interface cards are control processors for routing data for each service provider via line cards associated with that provider according to data paths).

Claim Rejections - 35 USC § 103

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claims 1-3, 6, 8, 11, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quiles et al. (US 7,065,072, hereafter Quiles), in view of Chiu et al. (US 6,597,689, hereafter Chiu).

12. For claim 1, Quiles discloses a telecommunications device for processing packet data received over a communications network, wherein the device includes a plurality of data processors (fig. 2, a lines card (such as items 70, 72) is read as a data processor), the device comprising:

a plurality of control processors (fig. 2, a network interface cards NIC 66 and 68), each control processor configured to manage data routing paths for routing the packet data through data processors in the plurality of data processors to destination on the network (col. 4 lines 37-44, a NIC routes data to a line card according to destination of the data); and

a plurality of logical nodes, wherein each logical node includes one or more data processors in the telecommunications device and is associated with a control processor in the plurality of control processor (col. 4, lines 58-67, a logical node is a plurality of line cards associated with a service provider, controlled by a NIC or control processor),

wherein each logical node is associated with a distinct network service provider (col. 4, lines 58-67, a logical node is a plurality of line cards associated with a service provider) and routes data for the network service provider routes data using the one or more data processors included in the logical node according to the data routing paths for routing data associated with each logical data processor (col. 4 lines 37-45 and 57-67, NIC routes data for line cards associated with an ISP according to data paths).

Quiles does not disclose the routing is according to the corresponding physical locations of the data processors in the telecommunications device.

However, Chiu discloses the routing is according to the corresponding physical locations of the data processors in the telecommunications device (fig. 3 and 5, switch card routes data for line cards according to line card slot number in a chassis, col. 26 lines 27-35, routing according to line card number).

Therefore, it would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Quiles and Chiu to route data according to physical location of line cards in a chassis to simplify system design and implementation.

13. For claim 6, Quiles discloses a telecommunications shelf for sending packet data to destination on a communications network including a plurality of slots configured to connect to data processors, the shelf comprising:

- a first logical shelf including a first set of one or more data processors, wherein each data processor in the first set is connected to a first set of one or more slots in the plurality of slots; and a second logical shelf including a second set of one or more data processors, wherein each data processor in the second set is connected to a second set of one or more slots in the plurality of slots (fig. 2, each line card is a data processor connected to a slot, col. 4 lines 37-67, line cards belonging to a provider is a logical shelf, there are 3 logical shelves for 3 providers),
- a first control processor separate from the first set of data processors configured to manage data routing paths through the first set of data processors and a

second control processor separate from the second set of data processors configured to manage data routing paths through the second set of data processors (col. 4 lines 39-45 and 58-67, network interface cards route data via line cards associated with each service provider according to data paths)

- wherein the first logical shelf is associated with a first network service provider that transfers data using the first set of one or more data processors and the second logical shelf is associated with a second network service provider that transfers data using the second set of one or more data processors (fig. 2, each line card is a data processor connected to a slot, col. 4 lines 37-67, line cards belonging to a provider is a logical shelf, there are 3 logical shelf for 3 providers).

Quiles does not disclose the routing is according to the corresponding physical locations of the data processors in the corresponding logical shelf.

However, Chiu discloses the routing is according to the corresponding physical locations of the data processors in the telecommunications device (fig. 3 and 5, switch card routes data for line cards according to line card slot number in a chassis, col. 26 lines 27-35, routing according to line card number).

Therefore, it would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Quiles and Chiu to route data according to physical location of line cards in a chassis to simplify system design and implementation.

14. For claim 2, Quiles discloses the invention as in claim 1. Quiles further discloses a power source configured to power the plurality of logical nodes (Chiu, fig. 3, power supply).

15. For claim 3, Quiles discloses the invention as in claim 1. Quiles further discloses a plurality of physical slots, wherein each of the plurality of data processors is coupled to a physical slot in the plurality of physical slots (Chiu, fig. 3, numbered physical slots with a line card in each).

16. For claim 8, Quiles-Chiu discloses the invention as in claim 7. Quiles-Chiu further discloses the first control processor is configured to manage data routing paths for the first entity and the second control processor is configured to manage data routing paths for the second entity (Quiles, col. 4 lines 39-45 and 58-67, network interface cards are control processors for routing data for each service provider via line cards associated with that provider according to data paths)

17. For claim 11, Quiles discloses the invention as in claim 11. Quiles further discloses comprising a power source configured to provide power to the first and second set of one or more data planes in the first and second logical shelves (Chiu, fig. 3, power supply).

18. For claim 17, Quiles-Chiu discloses the invention as in claim 1. Quiles-Chiu further discloses the packet data is formatted according to the OC3, OC12, OC148, Ethernet, or Gigabit Ethernet protocols (Chiu, fig. 5, OC3, T3, E3)

19. Claims 4, 9, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quiles-Chiu as applied to claim 3 and 6, and further in view of Van Doren (US 2001/0037435).

20. For claim 4, Quiles-Chiu discloses the invention as in claim 3. Quiles-Chiu does not disclose a data path from a first physical slot location to a second physical slot location in the device is mapped to a third physical slot location to a fourth physical slot location.

However, Van Doren discloses the same (fig. 5, [0007], [0011], [0013], a multiprocessor system that has common address space for multiple partitions or logical nodes, each comprising processors; routing messages are associated with a routing context which is looked up in a routing table to determine which physical location the corresponding processor can be found)

Therefore, it would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Quiles-Chiu and Van Doren to provide an efficient means for flexible configuration and partitioning in a computing system (Van Doren, [0010])

21. For claim 9, the claim is rejected for the same rationale as in claim 6. Quiles-Chiu does not disclose the first control processor is configured to map data routing paths based on a physical location of the data processors in the first set of data processors.

Van Doren discloses the first control processor is configured to map data routing paths based on a physical location of the data processors in the first set of data processors (Van Doren, [0047], an address mapping technique that uses logical ID of a logical partition QBB to translate starting address to physical location of a certain processor).

Therefore, it would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Quiles-Chiu and Van Doren to provide an efficient means for flexible configuration and partitioning in a computing system (Van Doren, [0010])

22. For claim 10, the claim is rejected for the same rationale as in claim 9.

23. Claims 13, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quiles as applied to claim 12, further in view of Chiu and Van Doren.

24. For claim 13, the claim is rejected for the same rationale as in claim 12. Quiles does not explicitly discloses receiving data associated with the first entity comprises receiving data for a first routing data path from a first location to a second location in the telecommunications device, and further comprising determining a third and fourth

location in the telecommunications device in which to route the received data, wherein routing the data comprises routing the data from a data processor in the third location to a data processor in the fourth location, the third and fourth data processors included in the first set of data processors

However, Chiu discloses multiple data processors in form of a slot array of line cards, each associated with a physical location (fig. 3).

Van Doren discloses an address mapping technique that uses logical ID of a logical partition QBB to translate address to physical location of a processor, for instance, mapping the first entity's first location to the third location and the first entity's second location to the fourth location, wherein the third and fourth locations are in one logical partition specifically for that entity (fig. 5, [0007], [0011], [0013], [0047]).

Therefore, it would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Quiles-Chiu and Van Doren to provide an efficient means for flexible configuration and partitioning in a computing system (Van Doren, [0010])

25. For claim 14, the claim is rejected for the same rationale as in claim 13.

Conclusion

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Falkenstein et al. US 7,016,379.
- Hughes et al. US 6,876,660.
- Cote. US 2003/0058854.
- Menon et al. US 2003/0103500.
- Chapman et al. US 7,113,484.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hieu T. Hoang whose telephone number is 571-270-1253. The examiner can normally be reached on Monday-Thursday, 8 a.m.-5 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on 571-272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HH

/Jeffrey Pwu/
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